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Chapter 1 : Cellonics Electronics Seminar Report Download -B-Tech Seminars

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Published on Dec 16, Abstract There is a saying in real estate; when land get expensive, multi-storied buildings are the alternative solution. We have a similar situation in the chip industry. For the past thirty years, chip designers have considered whether building integrated circuits multiple layers might create cheaper, more powerful chips. Performance of deep-sub micrometer very large scale integrated VLSI circuits is being increasingly dominated by the interconnects due to increasing wire pitch and increasing die size. Additionally, heterogeneous integration of different technologies on one single chip is becoming increasingly desirable, for which planar 2-D ICs may not be suitable. The three dimensional 3-D chip design strategy exploits the vertical dimension to alleviate the interconnect related problems and to facilitate heterogeneous integration of technologies to realize system on a chip SoC design. By simply dividing a planar chip into separate blocks, each occupying a separate physical level interconnected by short and vertical interlayer interconnects VILICs , significant improvement in performance and reduction in wire-limited chip area can be achieved. In the 3-Ddesign architecture, an entire chip is divided into a number of blocks, and each block is placed on a separate layer of Si that are stacked on top of each other. Motivation For 3-D ICs The unprecedented growth of the computer and the information technology industry is demanding Very Large Scale Integrated VLSI circuits with increasing functionality and performance at minimum cost and power dissipation. Continuous scaling of VLSI circuits is reducing gate delays but rapidly increasing interconnect delays. A significant fraction of the total power consumption can be due to the wiring network used for clock distribution, which is usually realized using long global wires. Additionally 3D ICs can be very effective large scale on chip integration of different systems. In 3D design architecture, and entire 2D chips is divided into a number of blocks is placed on separate layer of Si that are stacked on top of each other. For instance, logic gates on a critical path can be placed very close to each other using multiple active layers. This would result in a significant reduction in RC delay and can greatly enhance the performance of logical circuits. Since chip size directly affects the inter connect delay, therefore by creating a second active layer, the total chip footprint can be reduced, thus shortening critical inter connects and reducing their delay. The transistors on the Si surface are not actually packed to maximum density, but are spaced apart to allow metal lines above to connect one transistor or one cell to another. Next More Seminar Topics: Are you interested in this topic. Then mail to us immediately to get the full report.

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Chapter 2 : Download the Seminar Report for 3D IC's

This seminar report explains the concept of Three-dimensional Integrated Circuit or 3D IC. This is one of the emerging technologies that could revolutionize the electronic circuit design in future.

Types[edit] 3D ICs vs. Stacked memory die interconnected with wire bonds, and package on package PoP configurations interconnected with either wire bonds, or flip chips are 3D SiPs that have been in mainstream manufacturing for some time and have a well established infrastructure. PoP is used for vertically integrating disparate technologies such as 3D WLP uses wafer level processes such as redistribution layers RDL and wafer bumping processes to form interconnects. In all types of 3D Packaging, chips in the package communicate using off-chip signaling, much as if they were mounted in separate packages on a normal circuit board. One master die and three slave dies 3D SiCs[edit] The digital electronics market requires a higher density semiconductor memory chip to cater to recently released CPU components, and the multiple die stacking technique has been suggested as a solution to this problem. There is only one substrate, hence no need for aligning, thinning, bonding, or through-silicon vias. Process temperature limitations are addressed by partitioning the transistor fabrication to two phases. A high temperature phase which is done before layer transfer follow by a layer transfer use ion-cut , also known as layer transfer, which has been used to produce Silicon on Insulator SOI wafers for the past two decades. Follow by finalizing the transistors using etch and deposition processes. There are a number of key stacking approaches being implemented and explored. These include die-to-die, die-to-wafer, and wafer-to-wafer. Die-to-Die Electronic components are built on multiple die, which are then aligned and bonded. Thinning and TSV creation may be done before or after bonding. One advantage of die-to-die is that each component die can be tested first, so that one bad die does not ruin an entire stack. Die-to-Wafer Electronic components are built on two semiconductor wafers. One wafer is diced; the singulated dice are aligned and bonded onto die sites of the second wafer. As in the wafer-on-wafer method, thinning and TSV creation are performed either before or after bonding. Additional die may be added to the stacks before dicing. Wafer-to-Wafer Electronic components are built on two or more semiconductor wafers , which are then aligned, bonded, and diced into 3D ICs. Each wafer may be thinned before or after bonding. Vertical connections are either built into the wafers before bonding or else created in the stack after bonding. Moreover, the wafers must be the same size, but many exotic materials e. Benefits[edit] While traditional CMOS scaling processes improves signal propagation speed, scaling from current manufacturing and chip-design technologies is becoming more difficult and costly, in part because of power-density constraints, and in part because interconnects do not become faster while transistors do. This promises to speed up communication between layered chips, compared to planar layout. Footprint More functionality fits into a small space. Cost Partitioning a large chip into multiple smaller dies with 3D stacking can improve the yield and reduce the fabrication cost if individual dies are tested separately. This means that components can be optimized to a much greater degree than if they were built together on a single wafer. Moreover, components with incompatible manufacturing could be combined in a single 3D IC. Given that 3D wires have much higher capacitance than conventional in-die wires, circuit delay may or may not improve. Power Keeping a signal on-chip can reduce its power consumption by 10â€” times. Design The vertical dimension adds a higher order of connectivity and offers new design possibilities. Sensitive circuits may also be divided among the layers in such a way as to obscure the function of each layer. Bandwidth 3D integration allows large numbers of vertical vias between the layers. This allows construction of wide bandwidth buses between functional blocks in different layers. This arrangement allows a bus much wider than the typical or bits between the cache and processor. Cost While cost is a benefit when compared with scaling, it has also been identified as a challenge to the commercialization of 3D ICs in mainstream consumer applications. However, work is being done to address this. Although 3D technology is new and fairly complex, the cost of the manufacturing process is surprisingly straightforward when broken down into the activities that build up the entire process. By analyzing the combination of activities that lay at the base, cost drivers can be identified. Once the cost drivers are identified, it becomes a less complicated endeavor to determine where the majority

of cost comes from and, more importantly, where cost has the potential to be reduced. In order for 3D ICs to be commercially viable, defects could be repaired or tolerated, or defect density can be improved. This is an inevitable issue as electrical proximity correlates with thermal proximity. Specific thermal hotspots must be more carefully managed. Design complexity Taking full advantage of 3D integration requires sophisticated design techniques and new CAD tools. Depending on the technology choices, TSVs block some subset of layout resources. Via-last TSVs are manufactured after metallization and pass through the chip. Thus, they occupy both the device and metal layers, resulting in placement and routing obstacles. While the usage of TSVs is generally expected to reduce wirelength, this depends on the number of TSVs and their characteristics. It typically decreases for moderate blocks with modules and coarse block-level partitioning granularities, but increases for fine gate-level partitioning granularities. Aside from the massive overhead introduced by required TSVs, sections of such a module, e. This particularly applies to timing-critical paths laid out in 3D. Lack of standards There are few standards for TSV-based 3D IC design, manufacturing, and packaging, although this issue is being addressed. Heterogeneous integration supply chain In heterogeneously integrated systems, the delay of one part from one of the different parts suppliers delays the delivery of the whole product, and so delays the revenue for each of the 3D IC part suppliers. Design styles[edit] Depending on partitioning granularity, different design styles can be distinguished. Gate-level integration faces multiple challenges and currently appears less practical than block-level integration. It promises wirelength reduction and great flexibility. However, wirelength reduction may be undermined unless modules of certain minimal size are preserved. On the other hand, its adverse effects include the massive number of necessary TSVs for interconnects. This design style requires 3D place-and-route tools, which are unavailable yet. Also, partitioning a design block across multiple dies implies that it cannot be fully tested before die stacking. After die stacking post-bond testing , a single failed die can render several good dies unusable, undermining yield. This style also amplifies the impact of process variation , especially inter-die variation. In fact, a 3D layout may yield more poorly than the same circuit laid out in 2D, contrary to the original promise of 3D IC integration. Block-level integration This style assigns entire design blocks to separate dies. Design blocks subsume most of the netlist connectivity and are linked by a small number of global interconnects. Therefore, block-level integration promises to reduce TSV overhead. Sophisticated 3D systems combining heterogeneous dies require distinct manufacturing processes at different technology nodes for fast and low-power random logic, several memory types, analog and RF circuits, etc. Block-level integration, which allows separate and optimized manufacturing processes, thus appears crucial for 3D integration. Furthermore, this style might facilitate the transition from current 2D design towards 3D IC design. Basically, 3D-aware tools are only needed for partitioning and thermal analysis. This is motivated by the broad availability of reliable IP blocks. Also, critical paths can be mostly embedded within 2D blocks, which limits the impact of TSV and inter-die variation on manufacturing yield. Finally, modern chip design often requires last-minute engineering changes. Restricting the impact of such changes to single dies is essential to limit cost. Notable 3D chips[edit] In Tezzaron Semiconductor built working 3D devices from six different designs. Two wafers were stacked face-to-face and bonded with a copper process. The top wafer was thinned and the two-wafer stack was then diced into chips. For the 3D floorplan, designers manually arranged functional blocks in each die aiming for power reduction and performance improvement. Splitting large and high-power blocks and careful rearrangement allowed to limit thermal hotspots. The Teraflops Research Chip introduced in by Intel is an experimental core design with stacked memory. An academic implementation of a 3D processor was presented in at the University of Rochester by Professor Eby Friedman and his students. The chip runs at a 1.

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Chapter 3 : Technology Seminar | Flickr

3D IC technology 13D IC racedaydvl.com (Size: KB / Downloads:) What is 3D IC? In electronics, a three-dimensional integrated circuit (3D IC) is a chip in which two or more layers of active electronic components are integrated both vertically and horizontally into a single circuit.

Why do we need a three-dimensional 3D integration scheme now, rather than back in when Walter Shockley patented one of its key elements, the through-silicon via TSV? The answer is fivefold. First, using leading-edge 2DIC integration now only makes sense for the highest-margin, highest-volume designs. Unless you are going to be using millions of units, simply getting your design through the increasingly complex product qualification stage may provide you with more good die than you will ever need. Even if you were prepared to pay the premium to fabricate a small volume on a leading-edge process, you might not find a foundry to take on your design. According to an analysis by IBS, whereas a foundry was able to handle 60 to 80 new designs in the first year of offering its 65nm process, it may only be able to handle 12 to 16 designs in the first year of offering its 20nm process. Second, our ability to handle large amounts of multimedia data is being threatened by bandwidth limitations between packaged processors and memory. Fourth, power management is always an issue in modern systems design, and 3D integration can help with that, by shortening interconnects among the different die which, in turn, would reduce the need for global signal repeaters. And fifth, the yield of large die on leading-edge processes is usually lower than on more mature processes. Integrating several smaller, high-yielding die on a substrate using 3D techniques may offer a higher aggregate yield than putting all the functions on one large die. Tech Design Forum has covered this issue in detail in its Guide , but to recap: The silicon interposer routes the communication of the die with the package using vias that connect the microbumps on the top surface with the C4 bumps on the bottom surface. In a 3DIC, on the other hand, die are stacked on top of each other and interconnected by vias that go right through their substrates and connect with bumps on the surface of the next die down; the lowest die routes all the communication with the package - for itself as well as for the upper die. There are various combinations of these approaches, with some describing the use of a 3DIC stack, for example of memory die, alongside other die mounted on a silicon interposer as a 5. So what can we build with 2. Xilinx is using three or four smaller FPGA die rather than one huge one to improve its systemic yield, performance, and power, with the interposer providing around 10, interconnections between the FPGA die to mimic the connectivity possible in a monolithic solution. Options for a silicon photonic interface to complement the SerDes are said to be being explored. ST-Ericsson has showcased the architectural flexibility that 3D integration enables by rethinking the way it puts together a processor and its memory. The resultant 3DIC delivers a dramatic increase in bandwidth. Moving forward, there is much more to 3DIC than just implementation or verification, and we believe there are many more opportunities to extend the traditional EDA solutions to support this emerging technology. For example, virtual and fast prototyping is ideal for highly heterogeneous systems such as 3DIC; thermo-electromechanical simulation is also critical, and TCAD - while originally meant for process technology development - is an extremely powerful technology for modeling the thermo-electromechanical effects introduced by 3D structures. Longer term, we wil need pathfinding tools that can deal with the cost, performance, manufacturing, thermal, and test trade-offs, and help to assess whether a system-on-chip SoC , a system-in-package SiP or one of the many flavors of 3DIC integration is the most appropriate solution. With planar integration becoming increasingly difficult, exclusive and expensive, 3D strategies open up a rich alternative vein of opportunity for increasing functional integration - with all the benefits that has brought over the past half century.

Chapter 4 : Three-dimensional Integrated Circuit | 3D IC | Seminar Report

IEEE 64th -Orlando, FL, USA Suresh Ramalingam May 27 , 2ECTC 3D IC Background 3D IC Technology Development Summary Acknowledgements Outline Stacked Silicon Interconnect Technology refers to Xilinx 3D solutions.

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Chapter 5 : 3D IC Market Research Report- Global Forecast | MRFR

IDEA FOR 3D IC The large growth of computer and information technology industry is depending on VLSI circuits with increasing functionality and performance at minimum cost and power dissipation and 2D ICs generate various gate delays and interconnection delay.

Chapter 6 : Download the Seminar Report for 3D Printing

Explore 3- D IC's with Free Download of Seminar Report and PPT in PDF and DOC Format. Also Explore the Seminar Topics Paper on 3- D IC's with Abstract or Synopsis, Documentation on Advantages and Disadvantages, Base Paper Presentation Slides for IEEE Final Year Electronics and Telecommunication Engineering or ECE Students for the year

Chapter 7 : 3DIC: the advantages and challenges

This research papers examines the new technology ofHolographic Projections. It highlights the importance and need of this technology and how it represents the new wave in the future of technology and communications, the different application of the technology, the fields of life it will dramatically affect including business, education, telecommunication and healthcare.

Chapter 8 : PPT : 3 Dimensional Printing Seminar with Free Download

MonolithIC 3D Inc. is an IP company with operations in Silicon Valley, Romania and Israel. It invented and developed a practical path to the monolithic 3D Integrated Circuit, which includes multiple derivatives for Logic, Memory and Electro Optic devices.

Chapter 9 : Seminar report on 3d holographic p Presentations on authorSTREAM: Page 1

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